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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,914	10/29/2003	Gen Sasaki	244171US2 DIV	4524

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EXAMINER	
TRAN, NHAN T	
ART UNIT	**PAPER NUMBER**
2622	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/694,914	SASAKI, GEN	
	Examiner	Art Unit	
	Nhan T. Tran	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8,10 and 11* is/are allowed.

6)☒ Claim(s) *7 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 11/9/2006 have been fully considered but they are not persuasive.

The Applicant asserts:

(1) As to claim 9, Yoshihiro and Konishi fail to teach or suggest a real time processing unit having a pixel compensation function in which pixel data is multiplied by a predetermined pixel compensation parameter previously stored in a main memory that is configured to store generally processed pixel data outputted from the real time processing unit. Specifically, Yoshihiro fails to teach or suggest any predetermined compensation parameter previously stored in the DRAM 6 that is multiplied by each pixel data. Konishi also fails to teach or suggest a pixel compensation function in which each pixel data inputted sequentially is multiplied by a predetermined pixel compensation parameter previously stored in a main memory (Remarks, pages 9-11).

(2) As to claim 7, Yoshihiro and Hidari fail to teach or suggest a real time processing unit that is configured to perform a cumulative addition processing function in which a pixel data residing on a same position and a preceding frame of pixel data stored in the main memory is added to a corresponding pixel data in each frame inputted sequentially when the pixel data inputted sequentially extends multiple frames. In addition, Hidari does not teach or suggest any exceptional image processing

performed as a software program processing, which stores exceptionally processed pixel data in a main memory.

In response, the Examiner understands the Applicant's arguments but respectfully disagrees with the Applicant as follows:

(1) As disclosed by Yoshihiro, a real time processing unit 5 includes a real time processor 21 that performs a plurality of image processing operations such as AE, AF and AWB (automatic white balance) by reading parameters stored in a setup field of DRAM 6 as a work area. After performing AWB on the image data based on the setup parameters for white balance, the processed image is then stored back into an image section of DRAM 6. Paragraphs [0067] and [0024] disclose, *"an environmental setup for securing a field with DRAM of memory 6 in a work area, or each system of AF and AE-AWB carrying out an image processing field setup to the signal processor 21, or holding the image-processing data from the signal processor 21 on memory 6 is performed."* It is seen in Yoshihiro that the pixel compensation is AWB in which each pixel data is multiplied by a white balance parameter (note that AWB applies to all pixels of image data by inherency) stored in the setup field of DRAM 6. Further, Yoshihiro clearly discloses that the processed image data output from the processor 21 is also held by DRAM 6. Turning to Konishi reference, Konishi is relied upon for the teaching of a shading compensation that is not found in Yoshihiro. As taught by Konishi in col. 1, lines 10-14, 47-59 and col. 3, lines 50-65, in order to apply a shading compensation to each pixel, a shading correction factor that is preliminarily stored in a memory is multiplied to each pixel so as to compensate shading occurring due to nonuniformity in

illumination. Since the main memory has been taught by Yoshihiro as DRAM 6, Konishi is not relied for teaching of a main memory. The combination of Yoshihiro and Konishi therefore meets the claim limitations

(2) Hidari is not relied for teaching of exceptional image processing performed as a software program processing, which stores exceptionally processed pixel data in a main memory. Such software program processing has been taught by Yoshihiro as a JPEG compression program (Yoshihiro, paragraph [0033]). As seen in Hidari in Figs. 1 & 4 and col. 1, lines 45-51 and col. 8, line 44 – col. 9, line 15, the image data of a previous frame stored in a memory is added to the image data of a subsequent frame by accumulative addition processing for a number of times sequentially extending multiple frames for reducing noise (note Figs. 7 & 8 for a number of times of cumulative addition performed vs. rate of noise reduction). As such, each pixel data from the previous image *must* be added to a corresponding pixel at the same position in order for the accumulative addition in Hidari to function properly. Thus, the combined teachings of Yoshihiro and Hidari also meet the claim limitations of claim 7.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 10/19/2006 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Honma Yoshihiro (JP 10-042181) in view of Konishi (US 5,784,100).

Regarding claim 9, Yoshihiro discloses an image processing circuit (Figs. 1 & 2) configured to perform a predetermined image processing of pixel data in an image photographed by an image pickup device (CCD) (see Abstract), said circuit comprising:

a real time processing unit (processing circuit 5 including detailed processing section 21, Figs. 1 & 2) configured to sequentially input the pixel data photographed by said image pickup device, perform, by real time processing, a predetermined general image processing (i.e., AE, white balance, gamma corrections, etc.) of the inputted pixel data, and output the generally processed pixel data (paragraphs [0024] & [0030]-[0032] and [0066]-[0067]);

a main memory (either DRAM 6, Flash memory 7 or PC card 8) configured to store the generally processed pixel data outputted from said real time processing unit, in image frame units (paragraphs [0024]-[0025]);

central control unit (MPU 3) configured to execute exceptional image processing (JPEG compression) as a software program processing (JPEG compression software program) with respect to the stored generally processed pixel data, and store the

exceptionally processed pixel data in said main memory (see paragraphs [0033] and [0054]),

wherein said real time processing unit further comprises a pixel compensation function (automatic white balance function or AWB) in which each pixel data inputted sequentially is multiplied by a predetermined pixel compensation parameter (inherent white balance parameter) previously stored in said main memory (white balance parameter is stored in setup field of DRAM 6 as a work area for the processing unit to perform automatic white balance; also note the Examiner's response in section 1 above). See Figs. 1 & 2 and paragraphs [0049], [0066]-[0067].

Although Yoshihiro discloses automatic white balance (AWB), Yoshihiro does not disclose the predetermined pixel compensation including shading compensation. However, as taught by Konishi, an imaging apparatus includes a shading correction circuit that compensates shading occurring due to nonuniformity in illumination by multiplying the input image data with a shading correction factor to improve image quality (see Konishi, col. 1, lines 10-14, 47-59 and col. 3, lines 50-65).

Therefore, it would have been obvious to one of ordinary skill in the art to modify the imaging apparatus of Yoshihiro to include a pixel shading compensation function as taught by Konishi to compensate shading occurring due to nonuniformity in illumination by multiplying each pixel data inputted sequentially with a shading correction factor so as to improve image quality.

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Honma Yoshihiro (JP 10-042181) in view of Hidari (US 5,905,533).

Regarding claim 7, Yoshihiro discloses all limitations as analyzed in claim 9 (see claim 9) above *except* for disclosing that the real time processing unit is further configured to perform a cumulative addition processing function in which a pixel data residing on a same position in a preceding frame of pixel data stored in said main memory is added to a corresponding pixel data in each frame inputted sequentially when the pixel data inputted sequentially extends multiple frames, repeat the cumulative addition a predetermined number of times, and store results of the cumulative addition processing function in said main memory.

Hidari teaches a real time image processing unit (Figs. 1 & 4; unit 12) that has a cumulative addition processing circuit (23 or 3) to perform pixel addition by repeatedly adding pixel data of a previous frame stored in a memory into corresponding pixel data of a subsequent frame over and over again and store the results as cumulative image data into a memory (see Hidari, col. 5, lines 45-51 and col. 8, line 44 – col. 9, line 15). Hidari clearly shows that as the number of times of accumulative addition increases, the degree of noise is decreased (see Hidari, Figs. 7 & 8).

Therefore, it would have been obvious to one of ordinary skill in the art to enhance the real time processing unit of Yoshihiro in view of the teaching of Hidari to arrive at the Applicant's claimed invention by including a cumulative addition function for adding each pixel data of a previous frame into corresponding pixel data of a

subsequent frame for a predetermined of times by extending multiple frames in a sequential manner and then storing the cumulative image data into the main memory so as to reduce noises in the pixel data.

Allowable Subject Matter

5. Claims 8, 10 & 11 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding claim 8, the prior art of record fails to teach or fairly suggest the combination of all limitations required in claim 8 that includes **"...said weighting factor comprising a first factor to be multiplied to a pixel data residing at the same position in the preceding frame stored in said main memory, and a second factor to be multiplied to each corresponding pixel data in each frame inputted sequentially, a sum of said first and second factors being one."**

Regarding claims 10 & 11, these claim are allowed for the same reason provided in claim 8.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NHAN T. TRAN
Patent Examiner

DAVID OMETZ
SUPERVISORY PATENT EXAMINER